A Silicon Surface Code Architecture Resilient Against Leakage Errors

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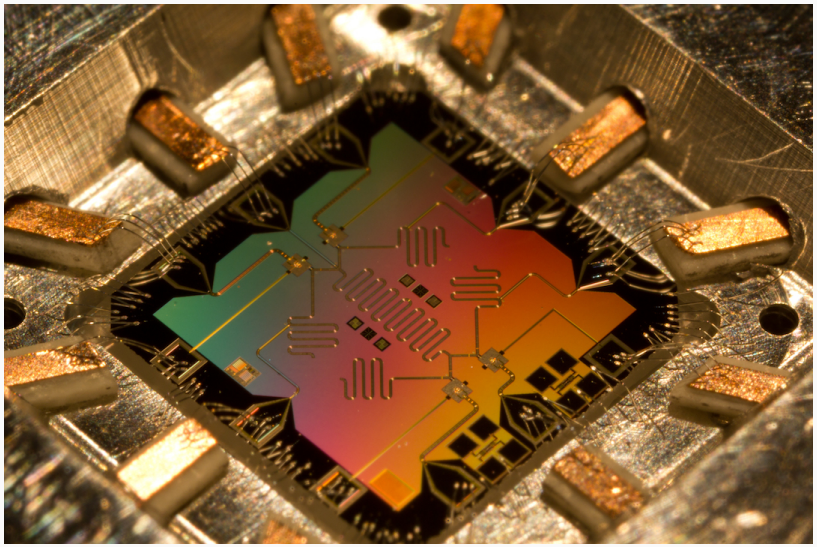
QEC19, August 2019

[1]University of Oxford, [2]University College London, [3]Quantum Motion Technologies Ltd

Silicon Spin Qubits

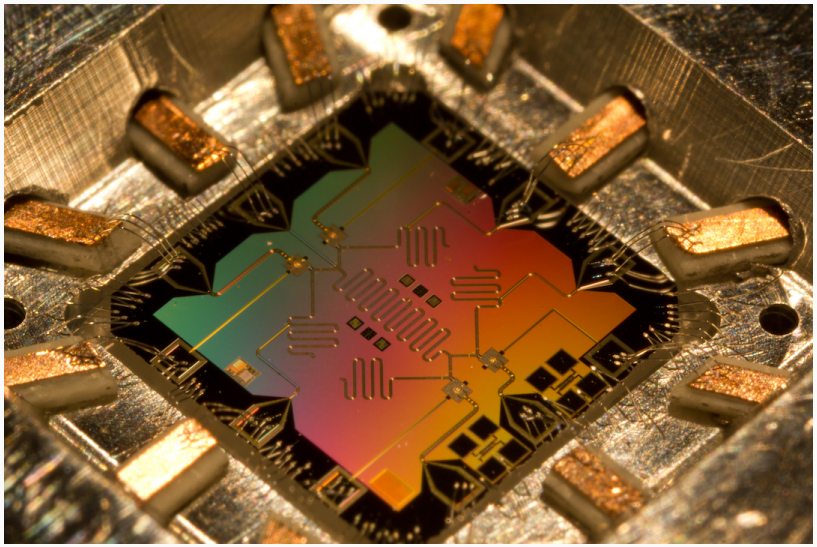
Quantum Computer Platforms

Quantum Computer Platforms



(a) Superconducting Qubits (Google)

Quantum Computer Platforms



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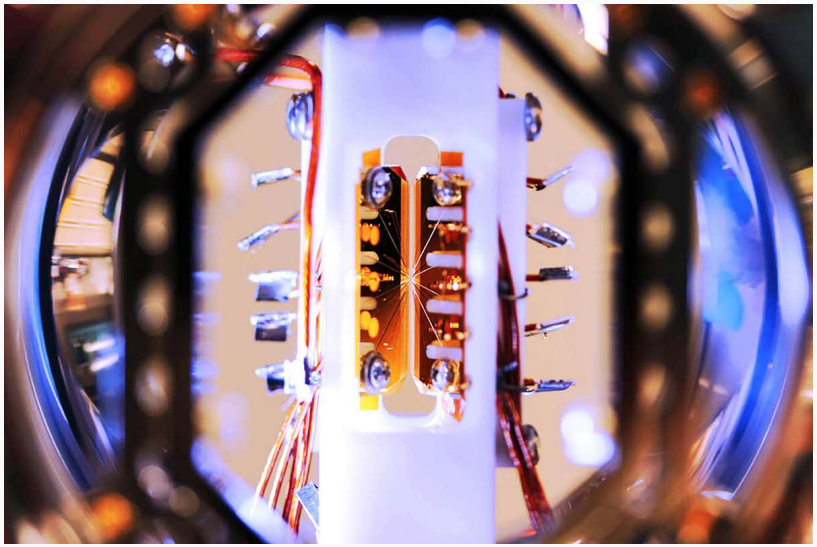
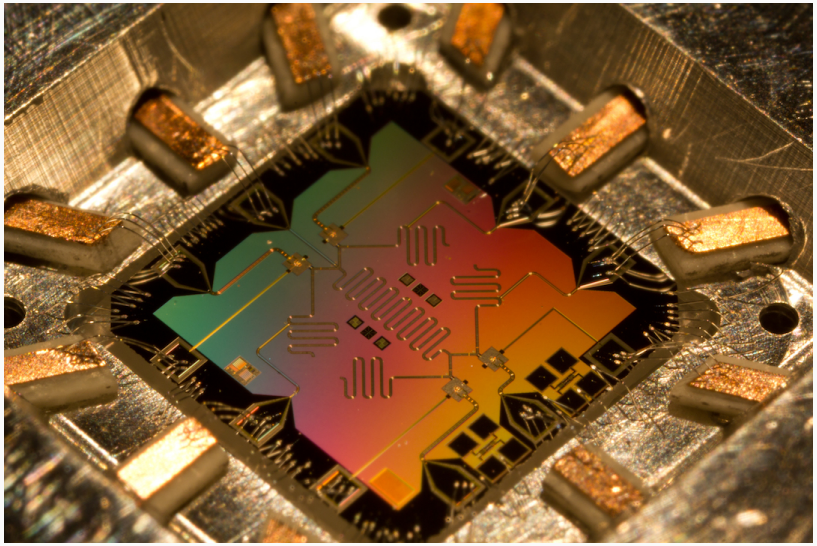


(b) Trapped Ion Qubits (UMD)

Quantum Computer Platforms



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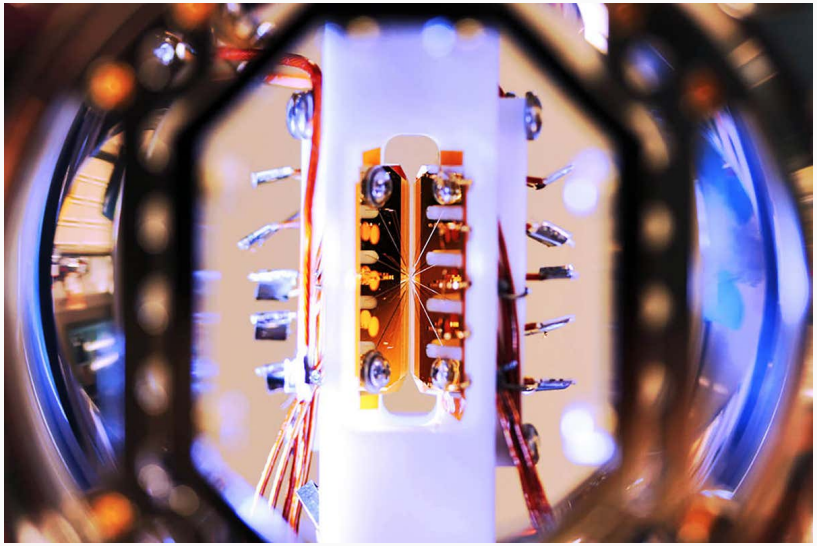

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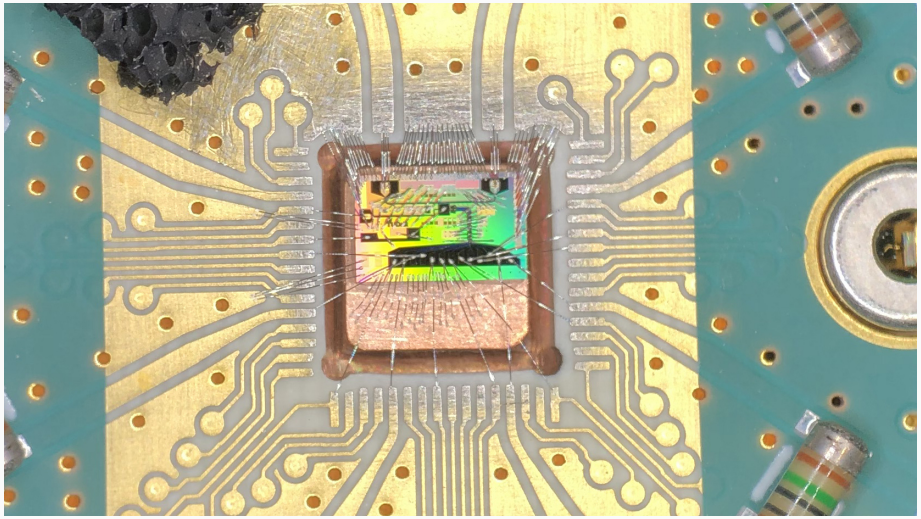


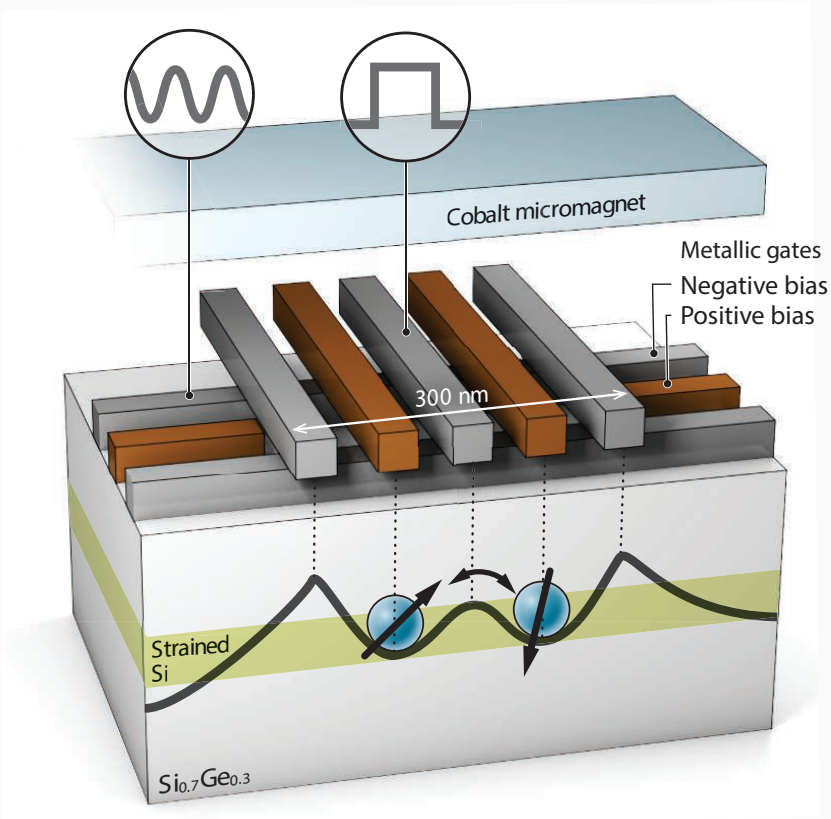
(c) Silicon Qubits (QuTech)

Silicon Quantum Dot Spin Qubits

- Mapping electron spin states to qubits

$$|\uparrow\rangle, |\downarrow\rangle \rightarrow |0\rangle, |1\rangle$$

- Such an isolated spin qubit can be created by trapping a single electron in the quantum dot.



[1] Image from Schreiber and Bluhm 2018

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Gate fidelity:

[1]Yang et al. 2019, [2]Huang et al. 2019, [3]Gidney and Ekera 2019

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Gate fidelity:

- Single-qubit gate: Exceed 99.9% [1]
- Two-qubit gate: $\sim$ 98% [2]

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Importance of scalability: 2048 bit Shor's factoring in 8 hours $\Rightarrow$ tens of millions of qubits [3]

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Surface Code

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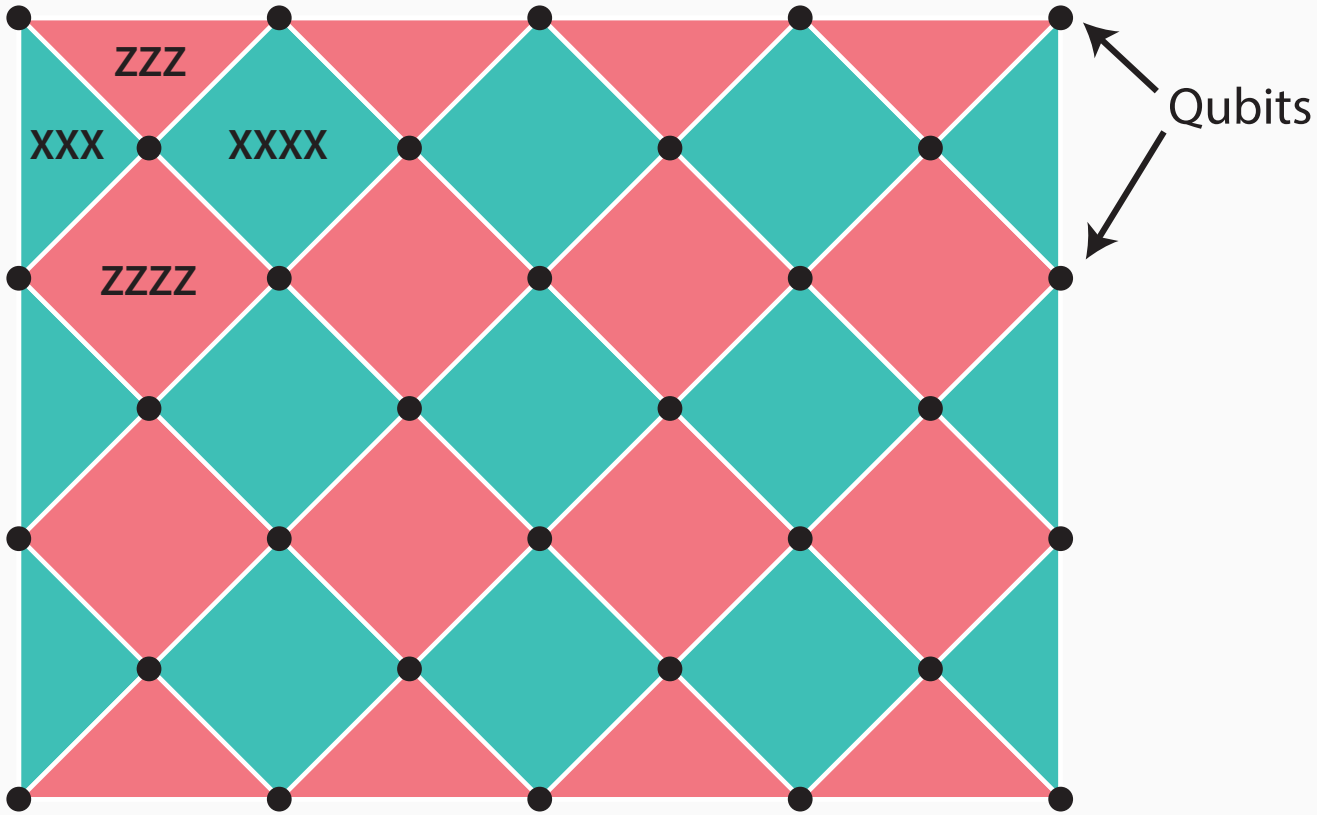

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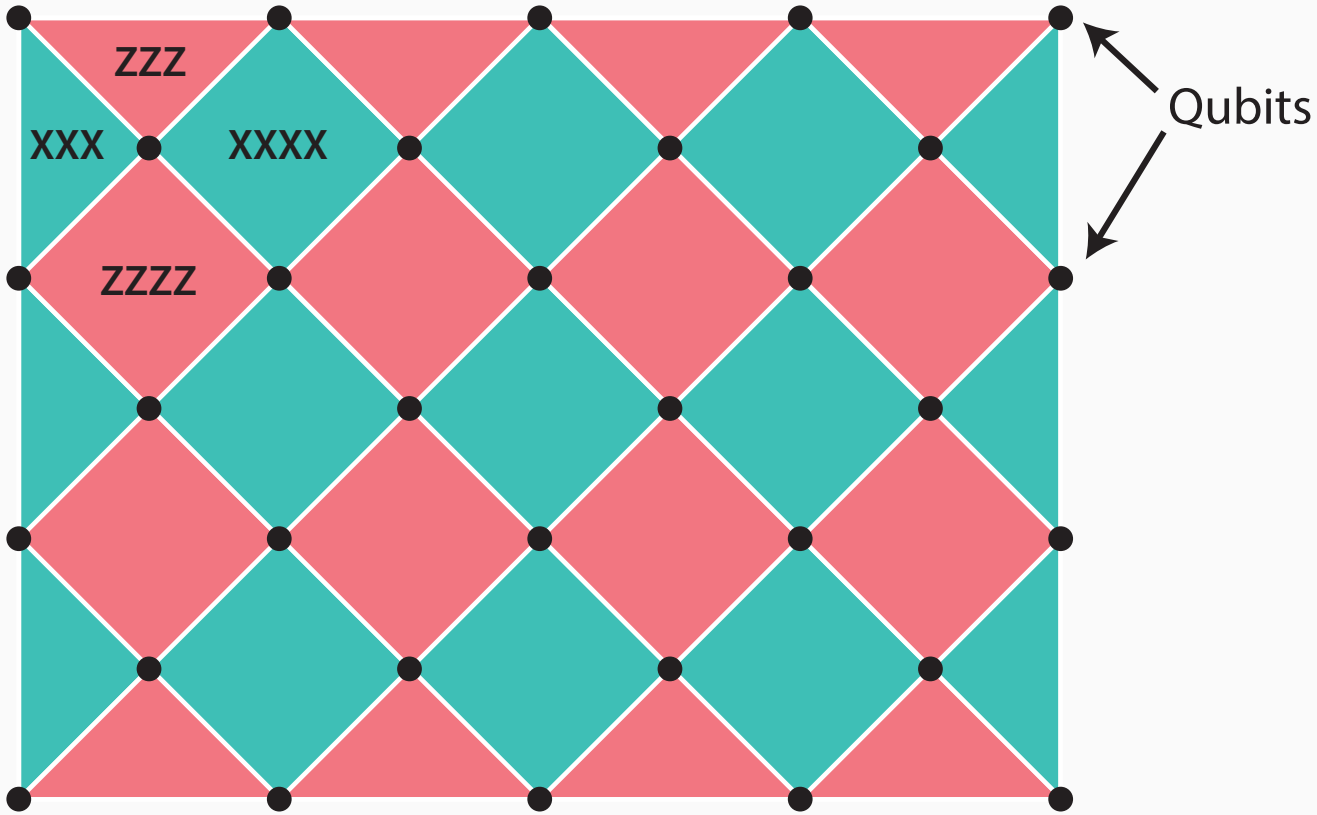
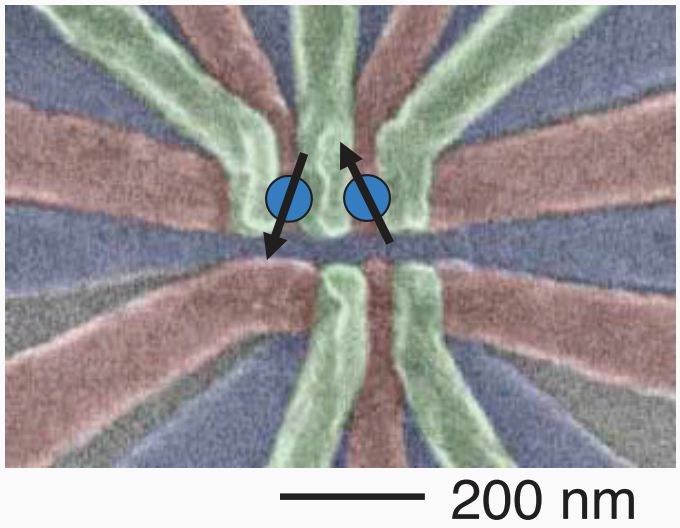


- Surface code is an error correction code that has one of the highest error threshold ($\sim 1\%$) using qubits in a 2D layout.
- It geometry is very favourable for silicon qubit fabrication.

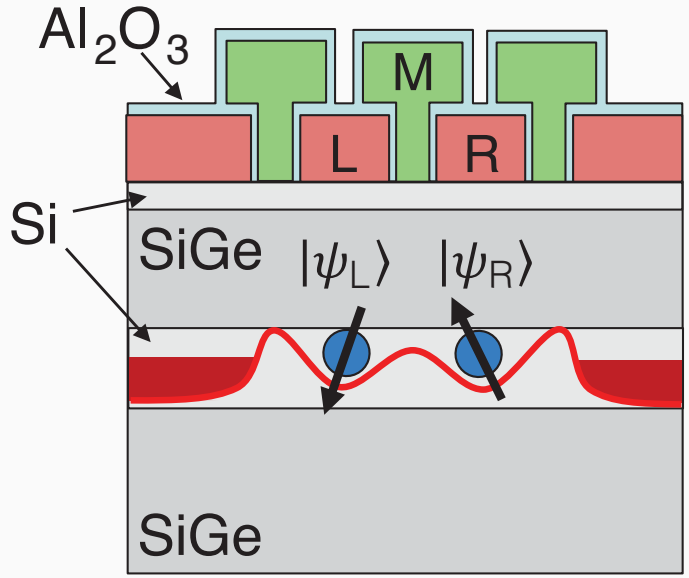
Challenges in Scaling-up

Challenges of scaling up

- **Dense packing of classical control lines.**



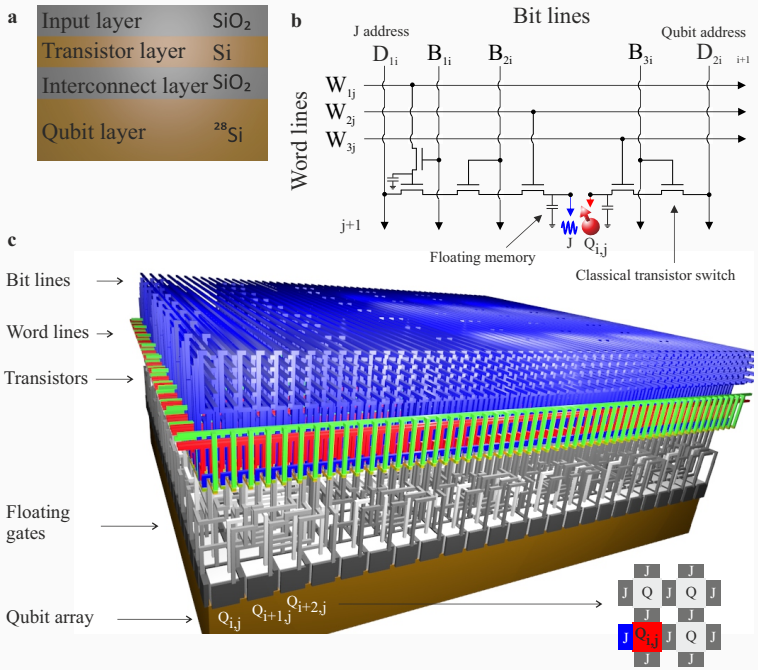
(a) Top View



(b) Side View

[1] Images from Zajac et al. 2018

Solution to Control Line Packing: Shared Control Lines



(a) Crossbar architecture[1]

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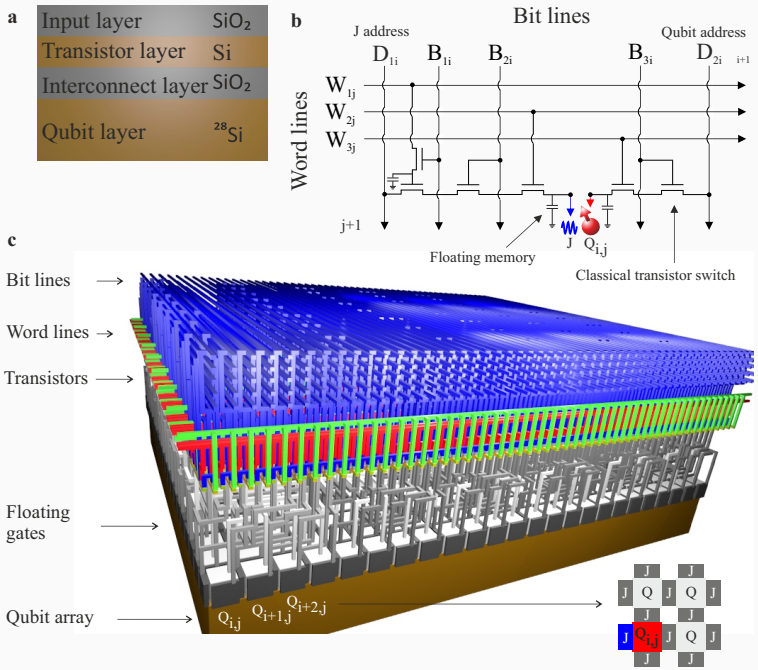
Solution to Control Line Packing: Shared Control Lines



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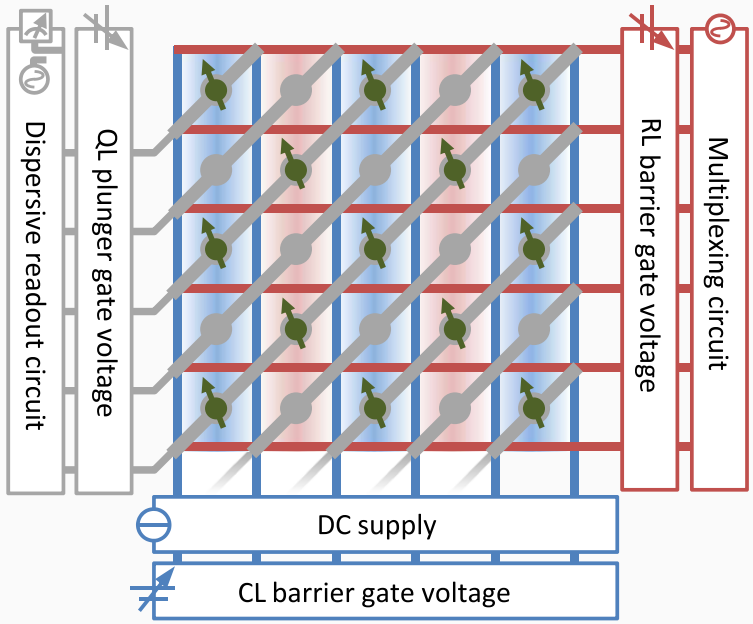

(b) Half-filled crossbar architecture[2]

[1]Veldhorst et al. 2017, [2]Li et al. 2018

Solution to Control Line Packing: Modular Architecture

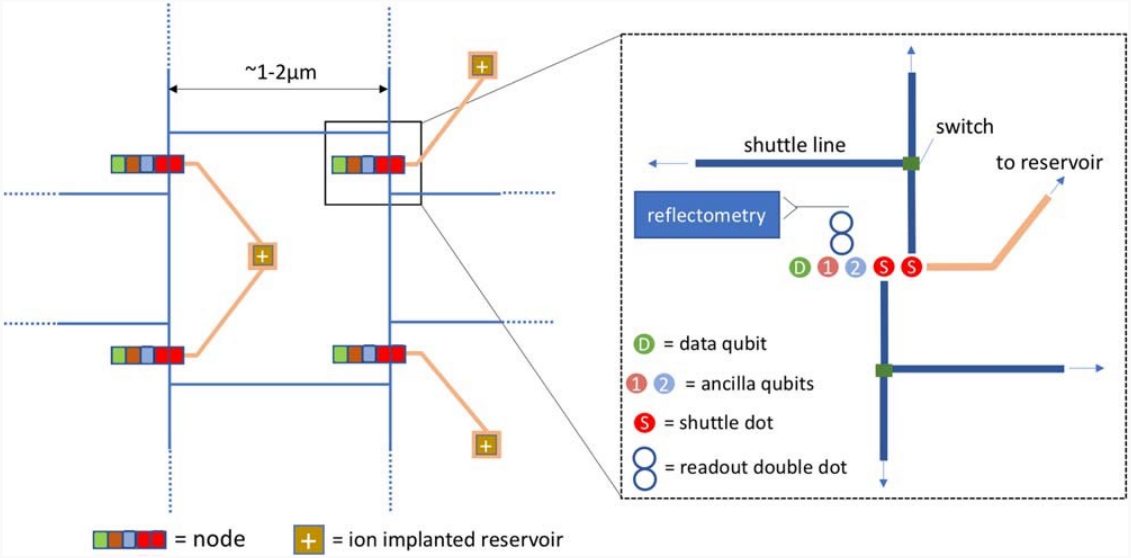

Figure 1: A modular network structure for silicon surface code [1]

[1] Buonacorsi et al. 2019

Leakage Error

- **Leakage error:** the quantum system escape out of the computational subspace that are used to defined the qubits.

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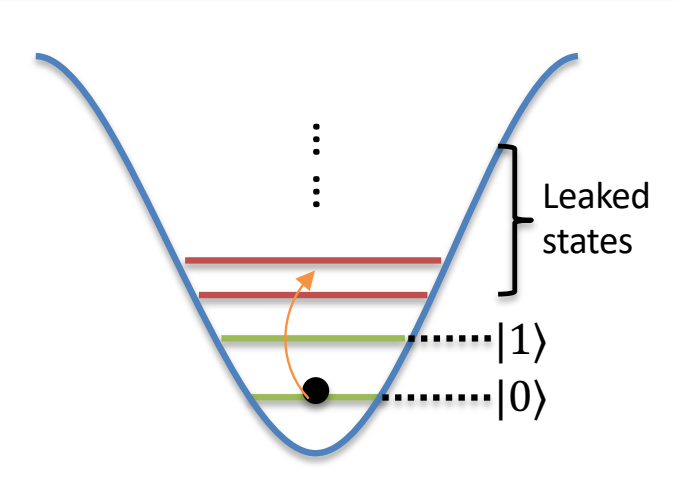
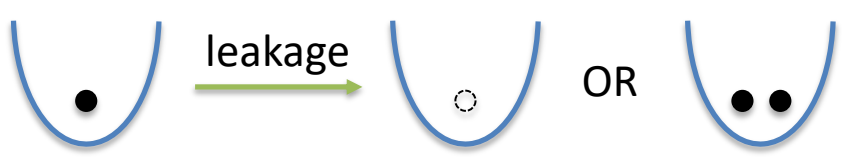
- **Leakage error:** the quantum system escape out of the computational subspace that are used to defined the qubits.
- In a superconducting qubit: leakage errors $\Rightarrow$ escaping out of the two lowest energy level.



- Similarly for trapped ion qubits.

Leakage Error in silicon

Single Electron Spin Qubits $\Rightarrow$ Charge Leakage Error:



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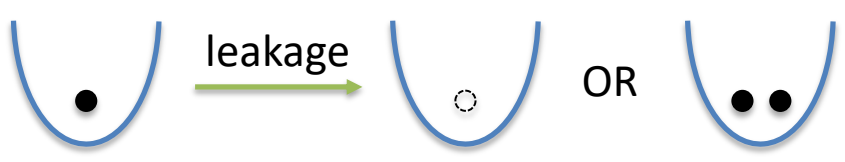
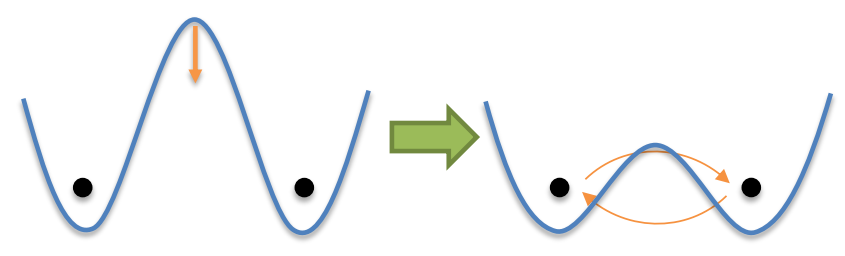
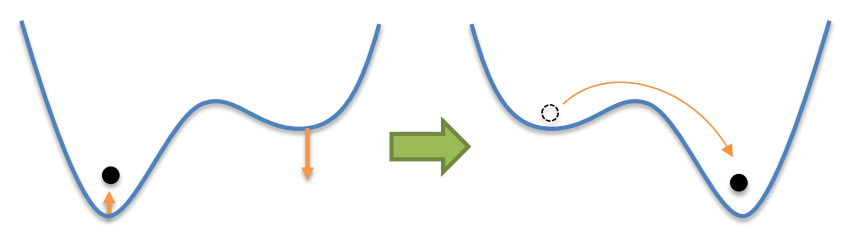


- Two-qubit gate:



- Shuttling:



Leakage Error

- **Leakage errors cannot be corrected by QEC code.**

  $\Longrightarrow$ accumulation of errors.

  $\Longrightarrow$ corrupting logical quantum information.

Leakage Detection

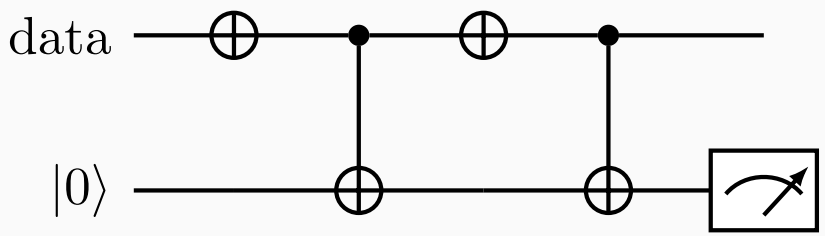
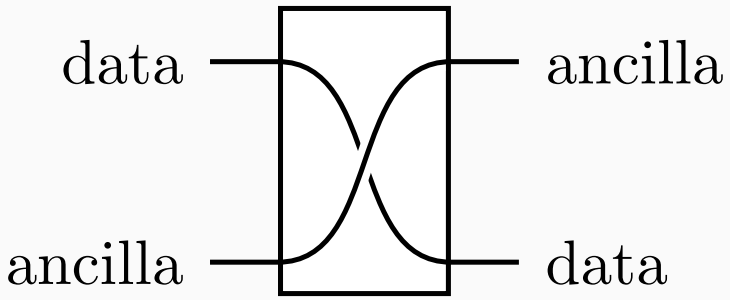


Figure 2: Leakage Detection Circuit.

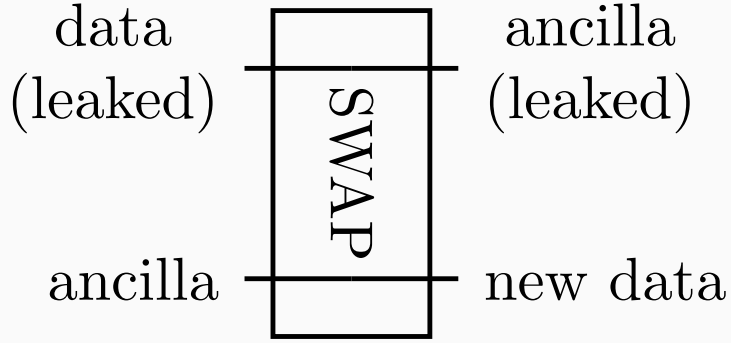
- Normal data qubit: ancilla flip once $\Rightarrow$ 1
- Leaked data qubit: ancilla does not flip $\Rightarrow$ 0

[1]Preskill 1998, [2] Gottesman Ph.D Thesis

Leakage Reduction



(a) Normal Qubit



(b) Leaked Qubit

[1]Aliferis and Terhal 2007, [2]Fowler 2013, [3] Suchara et al. 2015

Limitation of Existing Leakage Fixing Circuits

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- **Assuming two-qubit gates do not transfer leakages:**

  Does not apply to charge leakage errors in silicon.

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- **Assuming two-qubit gates do not transfer leakages:**

  Does not apply to charge leakage errors in silicon.

- **How to restored the left-over leaked qubits:**

  Hard to fit charge reservoirs next to every dot in a dense quantum dot array for *restoring leakage* in silicon.

Challenges in scaling up silicon qubits

- **How to fit in the control lines**
- **How to restore leakage errors**

Our Solution

Our architecture

- **How to fit in all the control lines**
- **How to restore leakage errors**

Our architecture

Introduce elongated mediator quantum dots to mediate two-qubit interaction.

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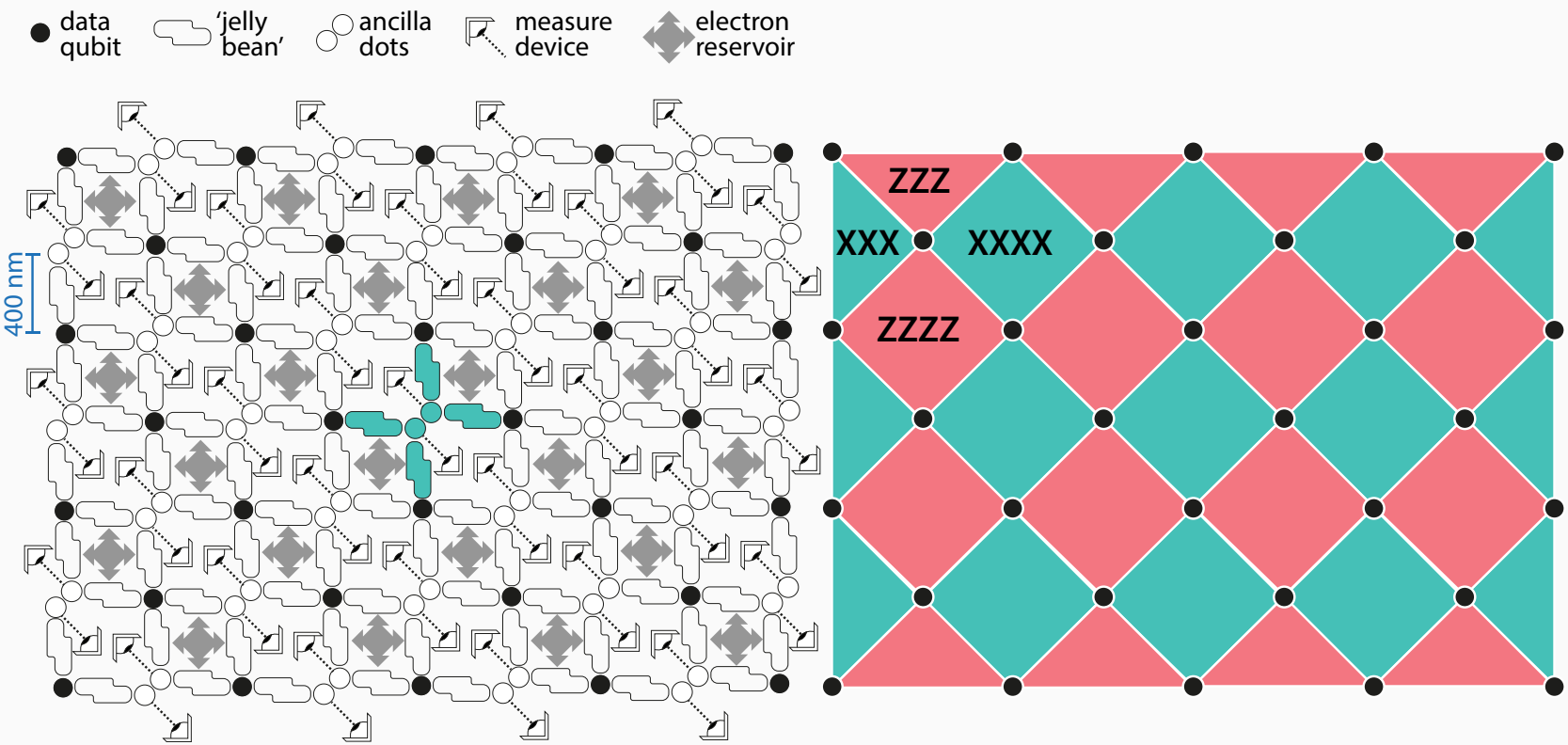
- **How to fit in all the control lines** : provide *extra spaces* for classical control lines and charge reservoirs.
- **How to restore leakage errors**

Our architecture

Introduce elongated mediator quantum dots to mediate two-qubit interaction.

- **How to fit in all the control lines** : provide *extra spaces* for classical control lines and charge reservoirs.
- **How to restore leakage errors** : use the electrons in the mediator to *restore the leakage in the qubits in real time*.

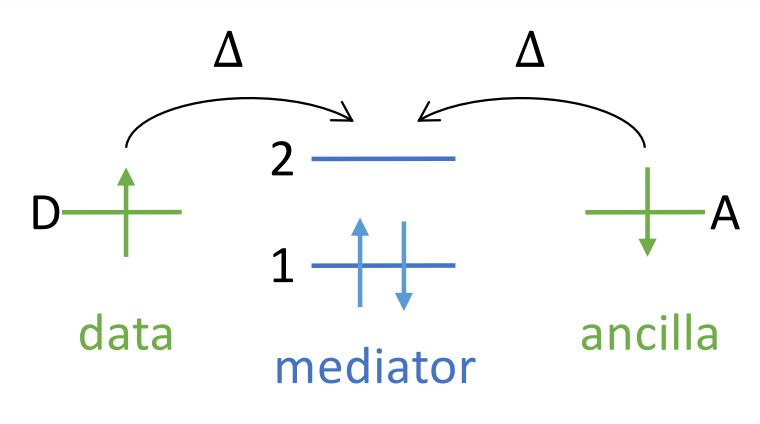
Our architecture



(a) Physical Layout

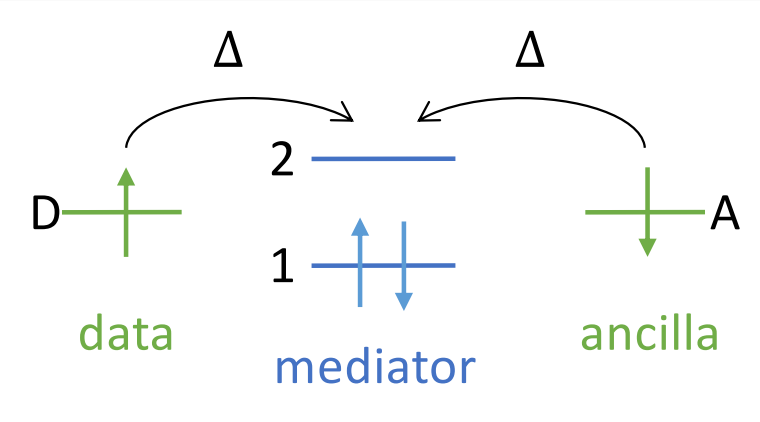
(b) Surface Code

Mediated Exchange Interaction



(a) Mediated interaction

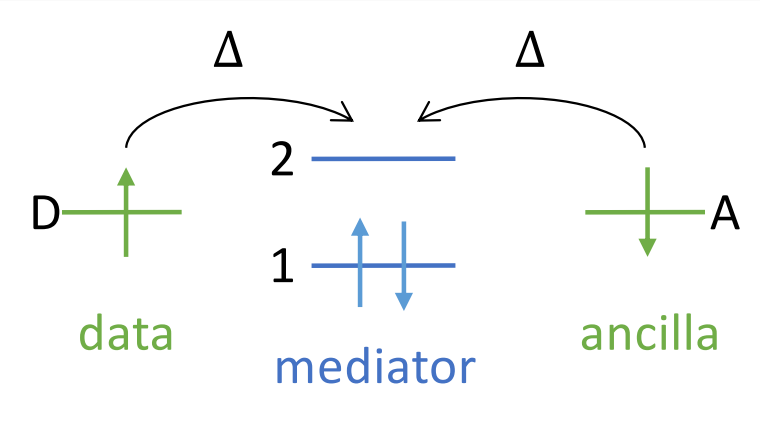
Mediated Exchange Interaction



(a) Mediated interaction

- Interaction strength $\propto \frac{1}{\Delta^2}$

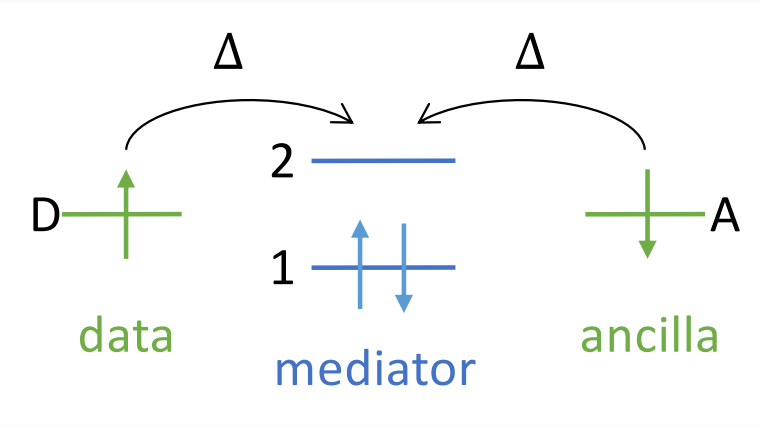
Mediated Exchange Interaction



(a) Mediated interaction

- Interaction strength $\propto \frac{1}{\Delta^2}$
- Turn on interaction: decrease $\Delta \Rightarrow$ align mediator energy level.

Mediated Exchange Interaction



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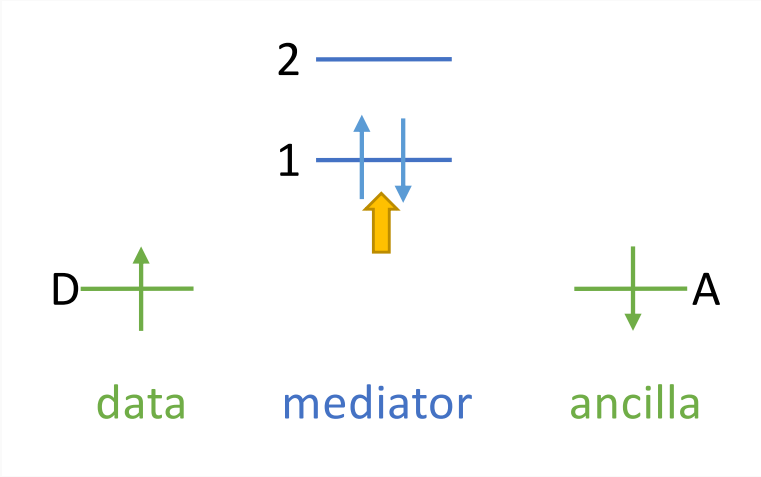


(b) Turn off interaction

- Interaction strength $\propto \frac{1}{\Delta^2}$
- Turn on interaction: decrease $\Delta \Rightarrow$ align mediator energy level.
- Turn off interaction: increase $\Delta \Rightarrow$ raise mediator energy level.

Leakage Restoration

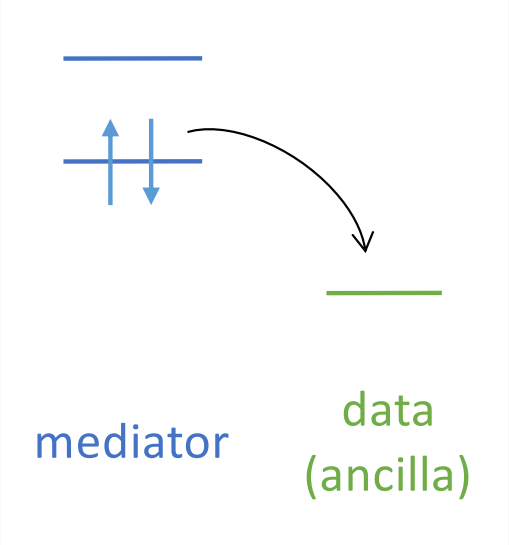


Figure 3: Restoration of leakage via mediators.

- Relaxation time scale (~ 10 ns) $\ll$ other operations (μs).
- e-e repulsion in qubit dots $\gg$ energy scale of other operations.

Leakage Restoration

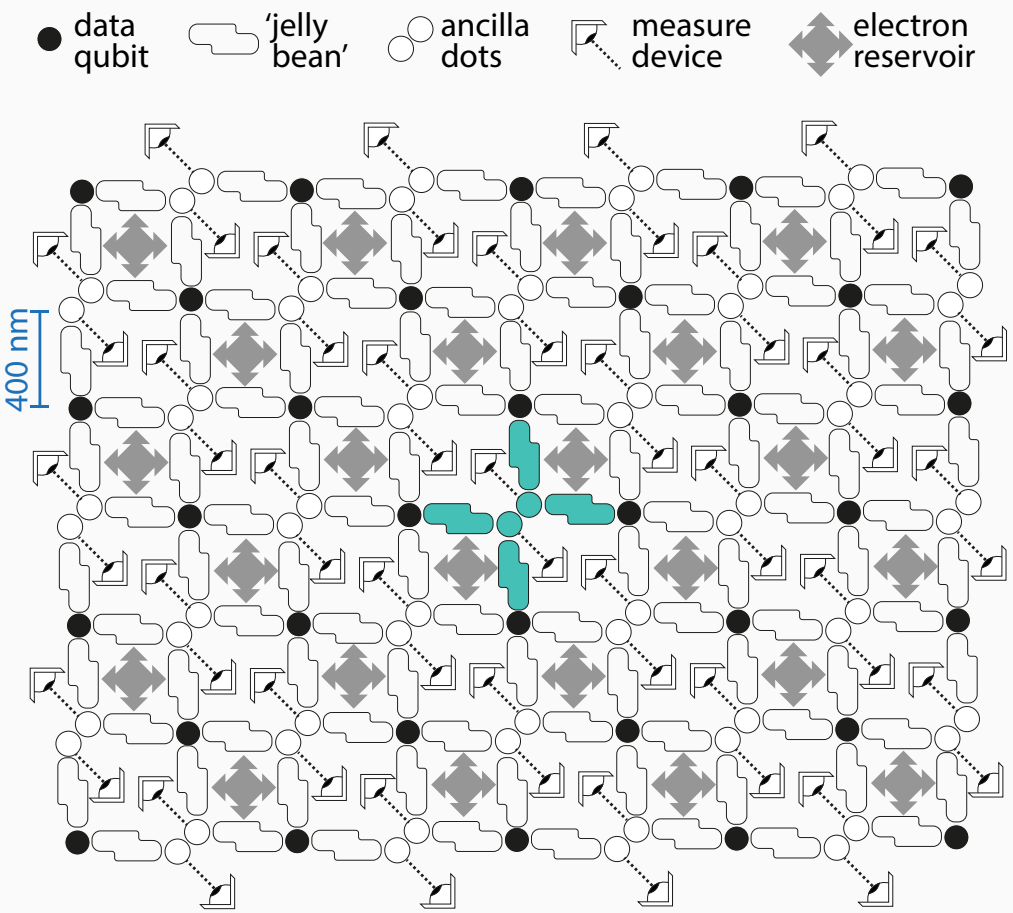
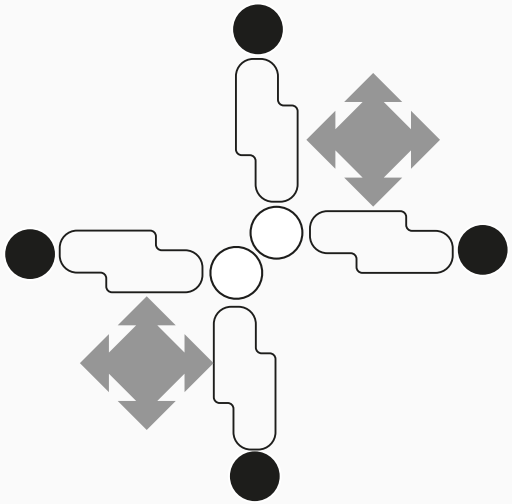


Figure 4: Architecture layout

Leakage Restoration



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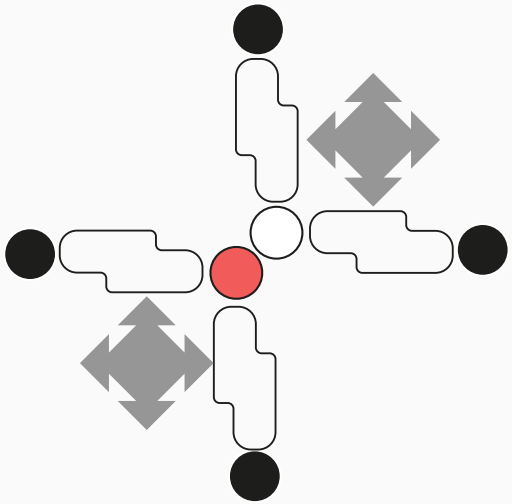

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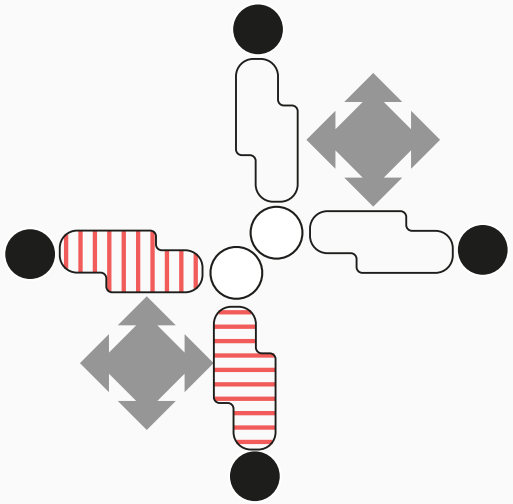

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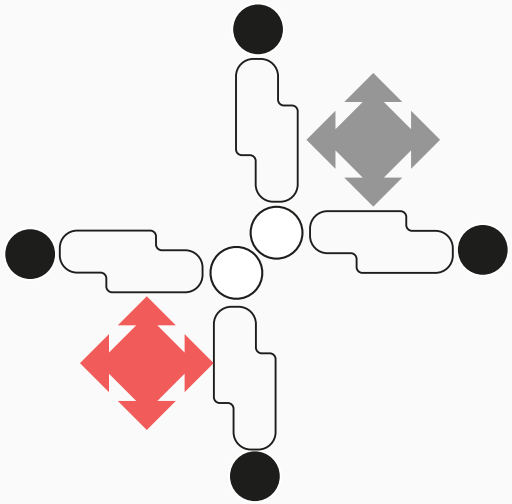

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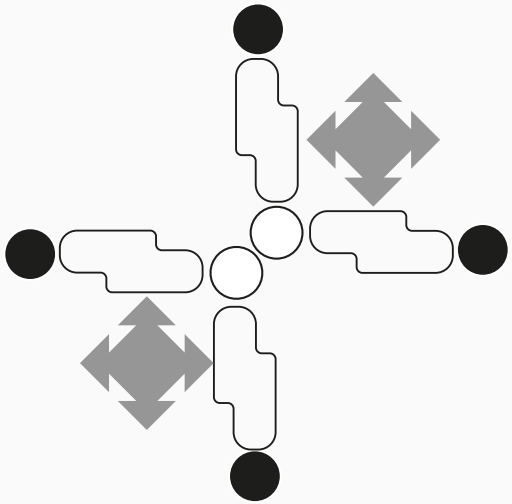
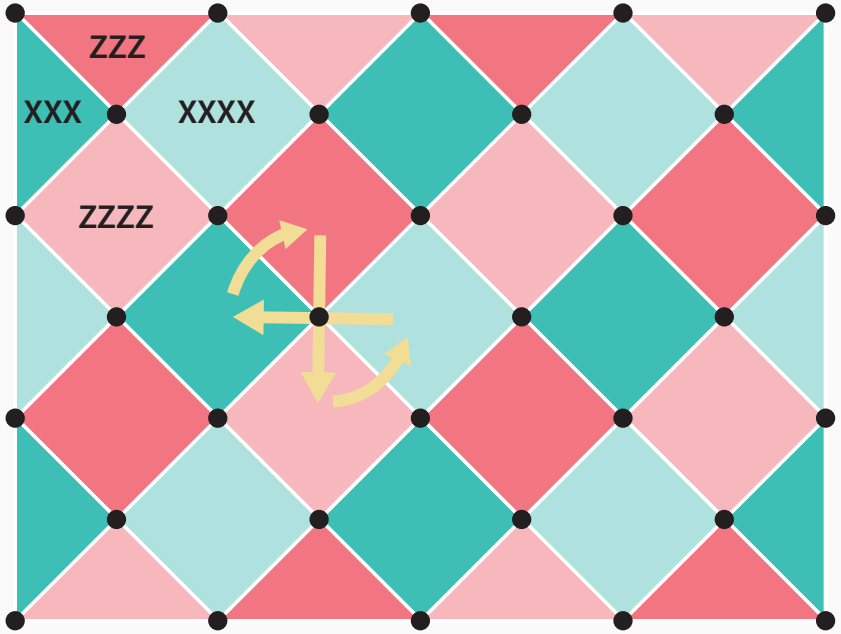


Surface Code Partitions



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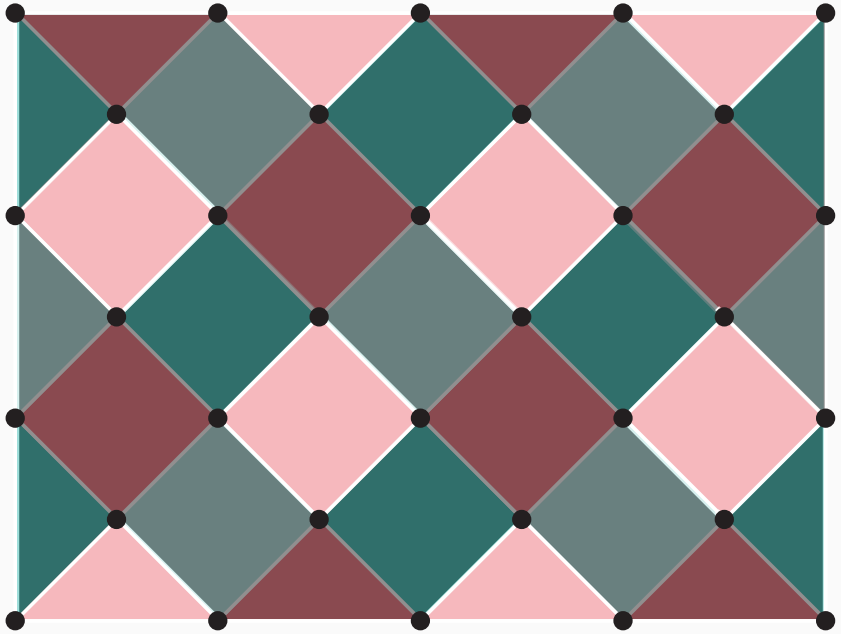

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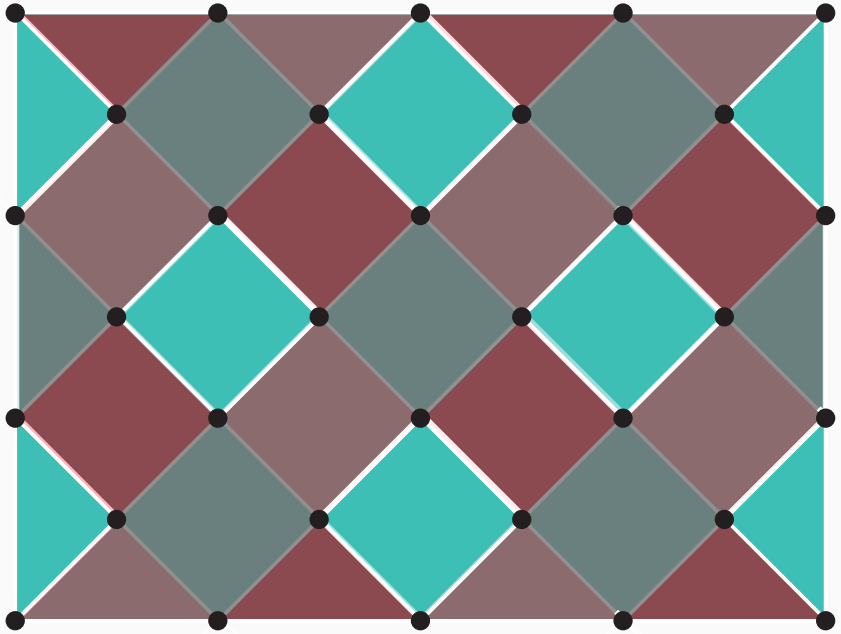

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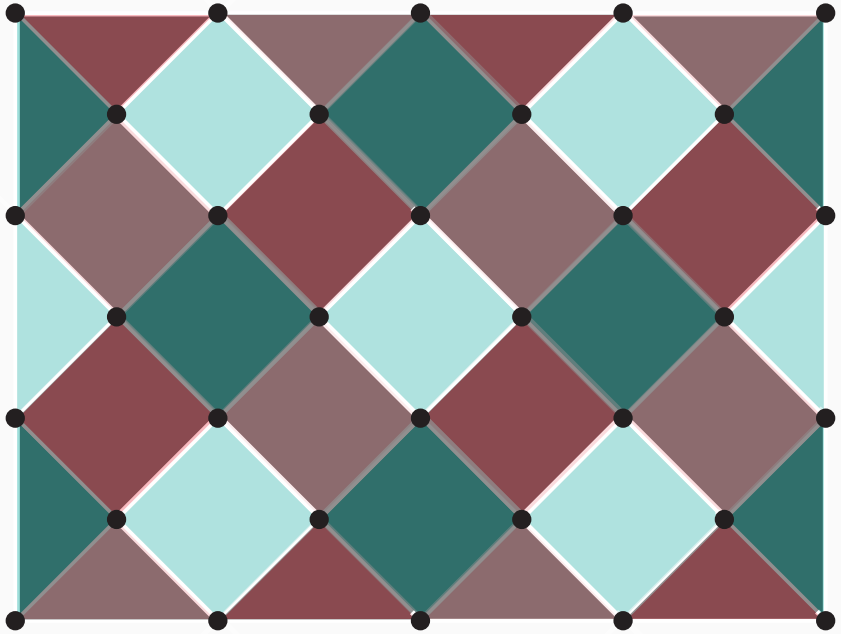

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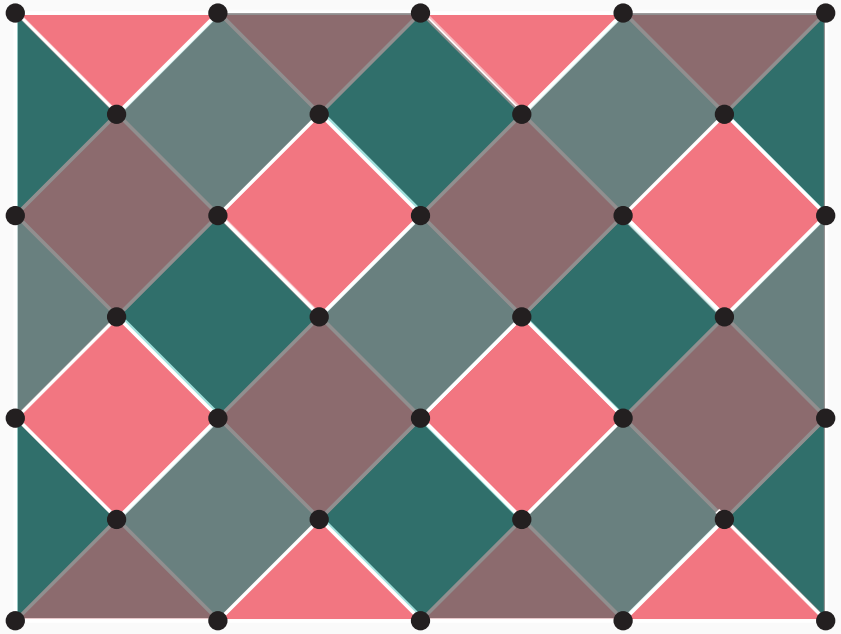

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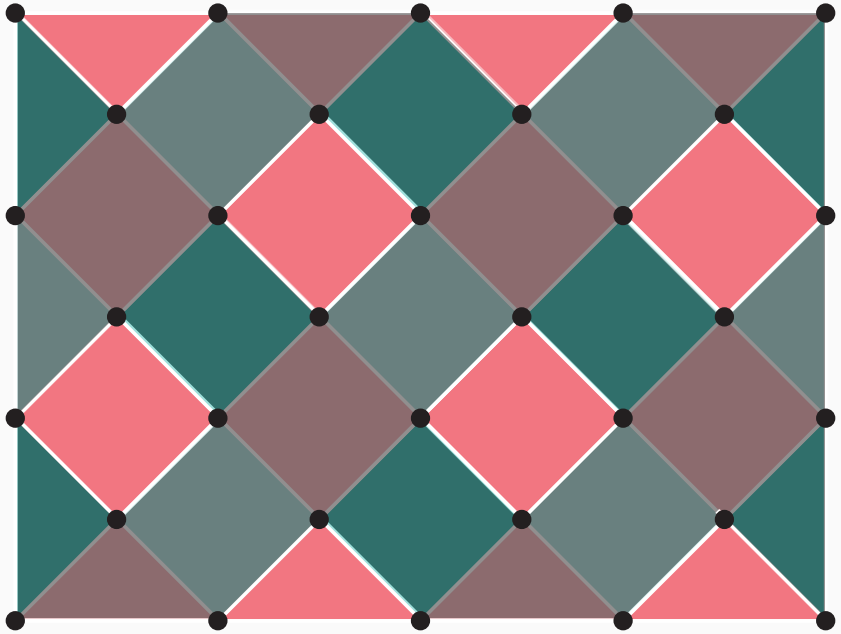
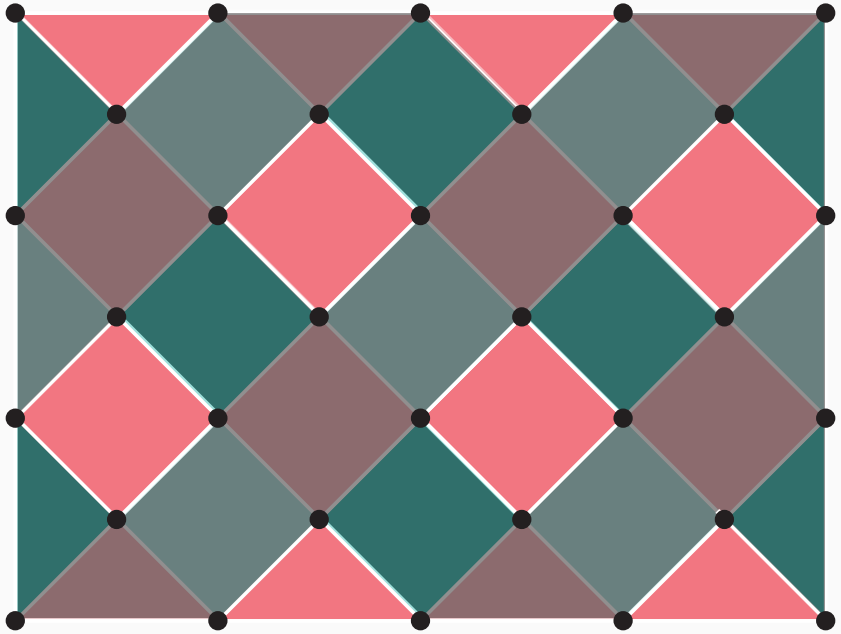


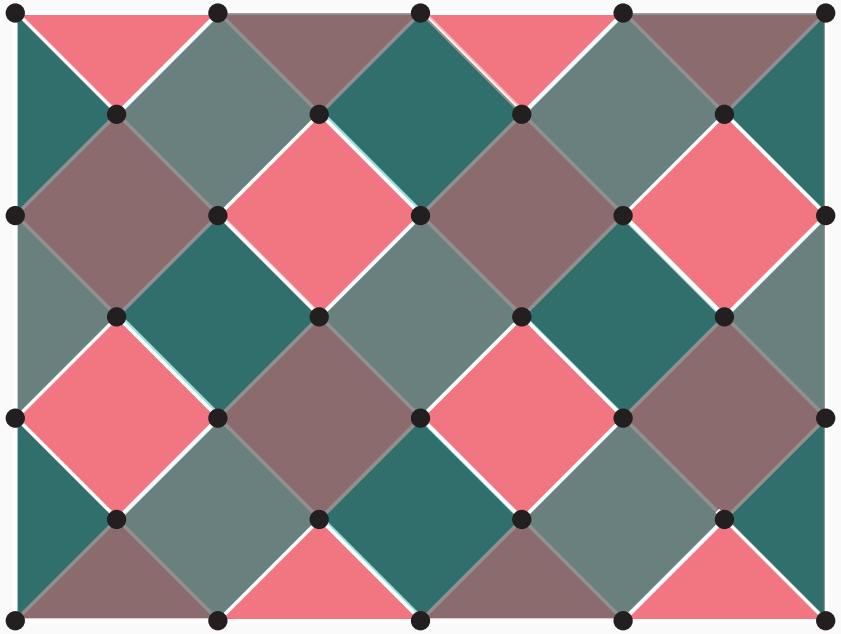
- Isolated plaquettes within each partition.

Surface Code Partitions



- Isolated plaquettes within each partition.
- Reset inactive partitions.

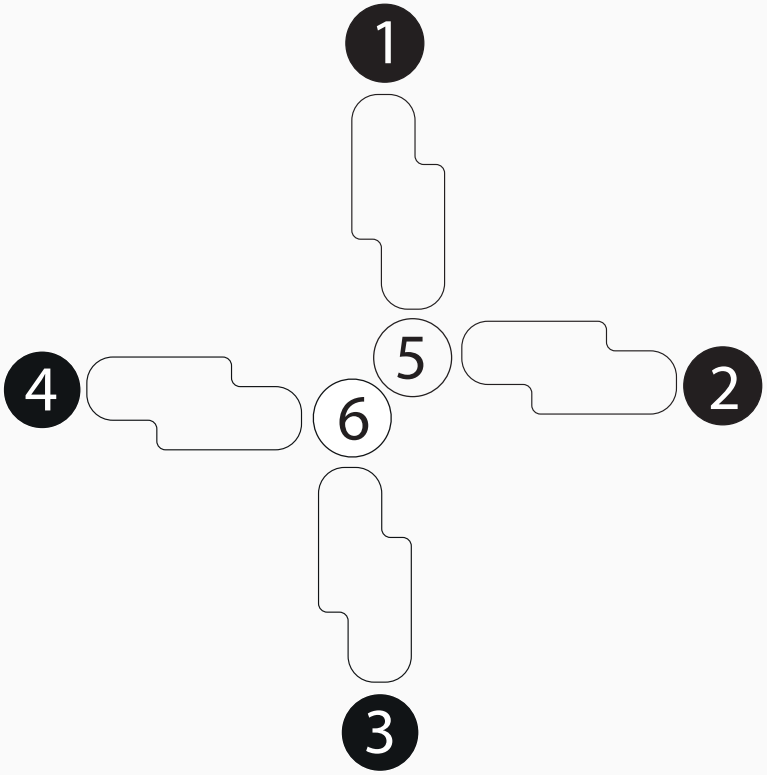
Surface Code Partitions



- Isolated plaquettes within each partition.
- Reset inactive partitions.

$\Rightarrow$ Leakage errors will be contained within individual plaquette.

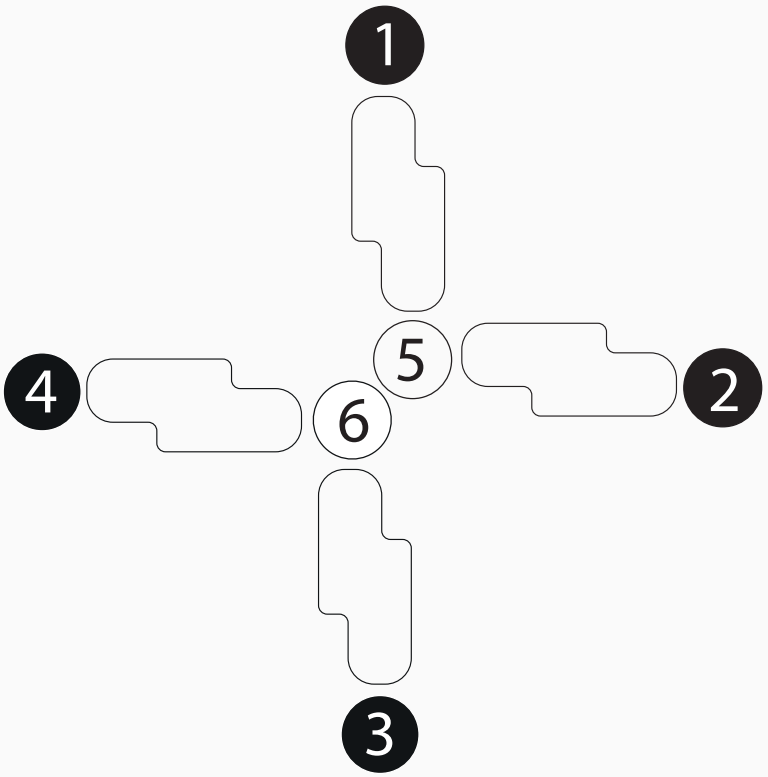
Stabiliser Check



(a) Physical layout

Double-dot ancilla: [1]Jones et al. 2018, [2]Veldhorst at al. 2017

Stabiliser Check



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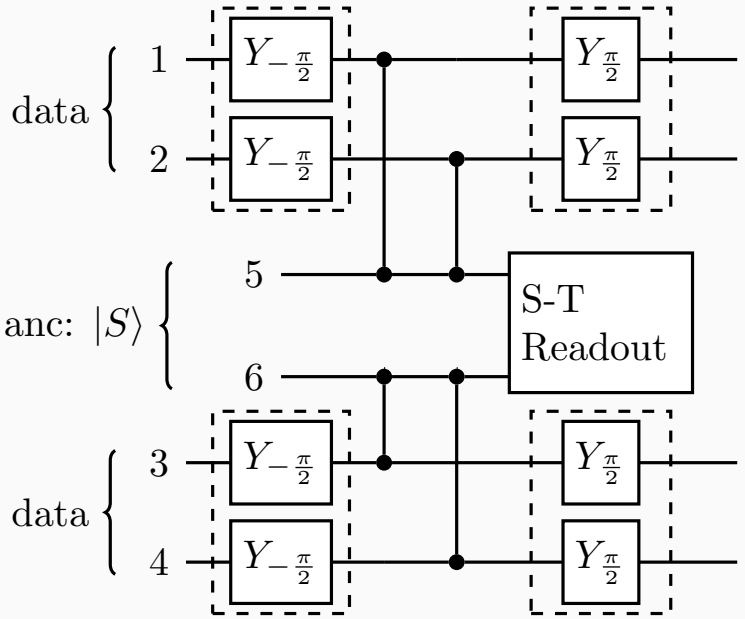

(b) The Stabiliser Check Circuit

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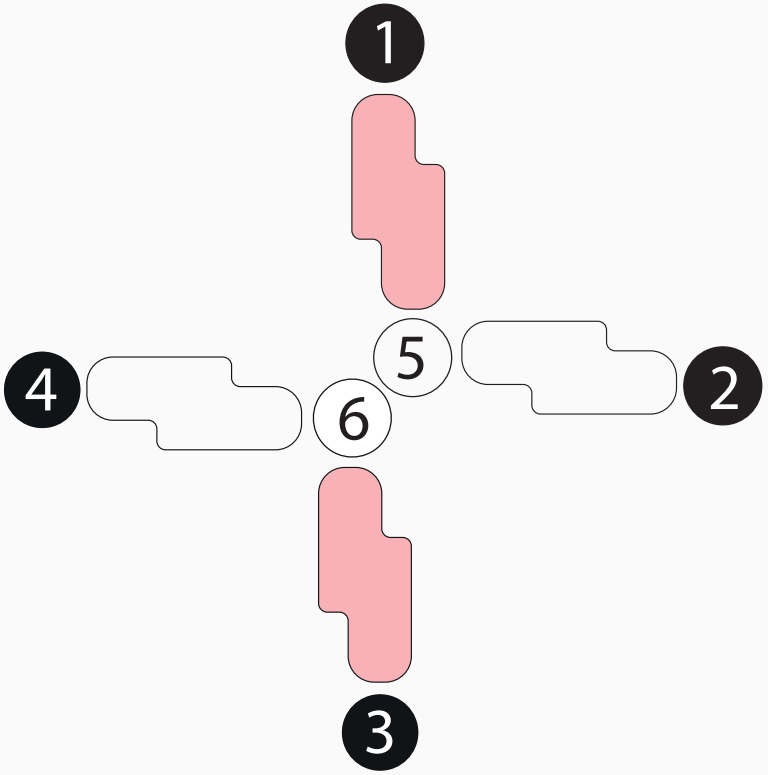

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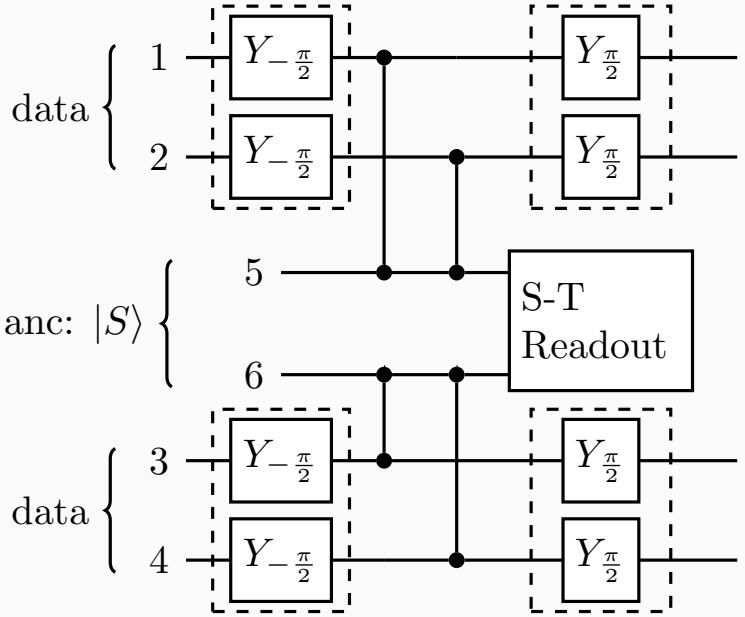

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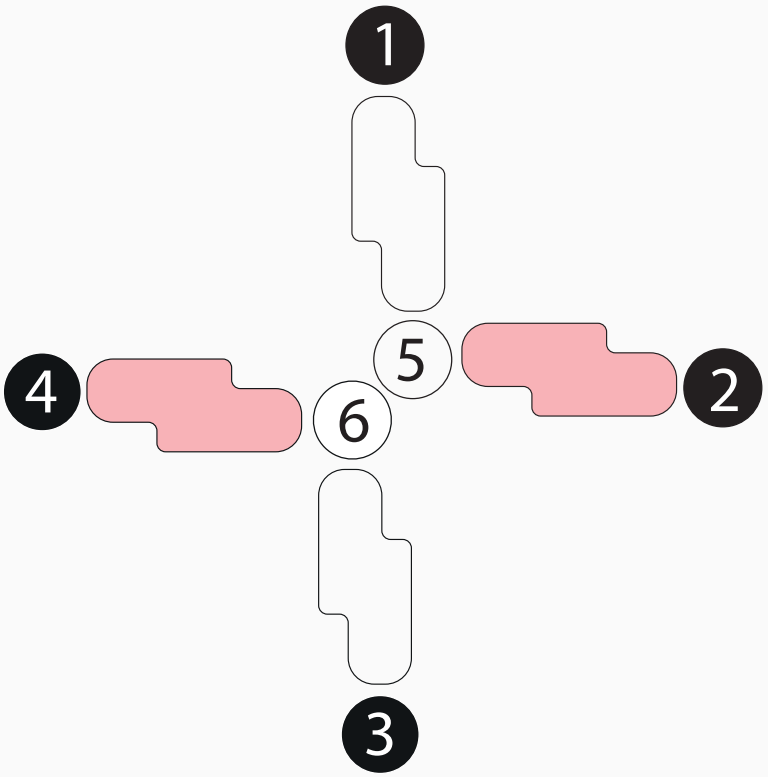
Stabiliser Check



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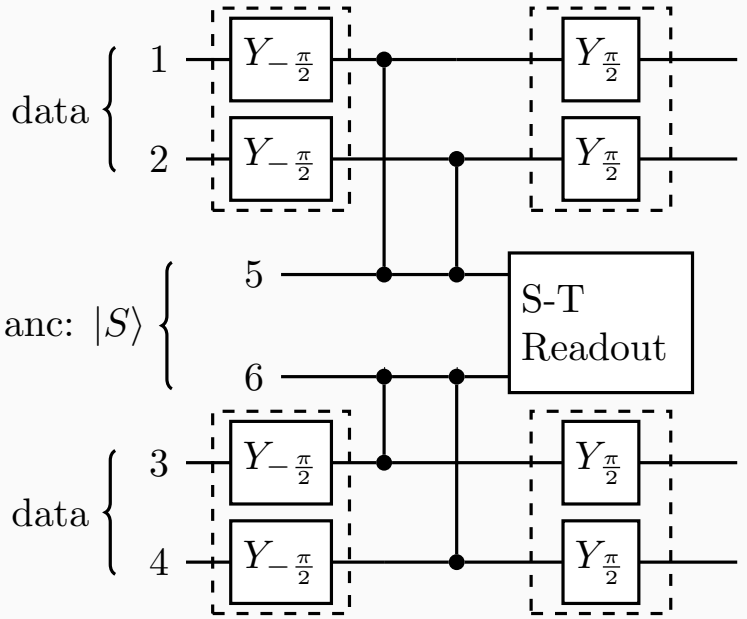

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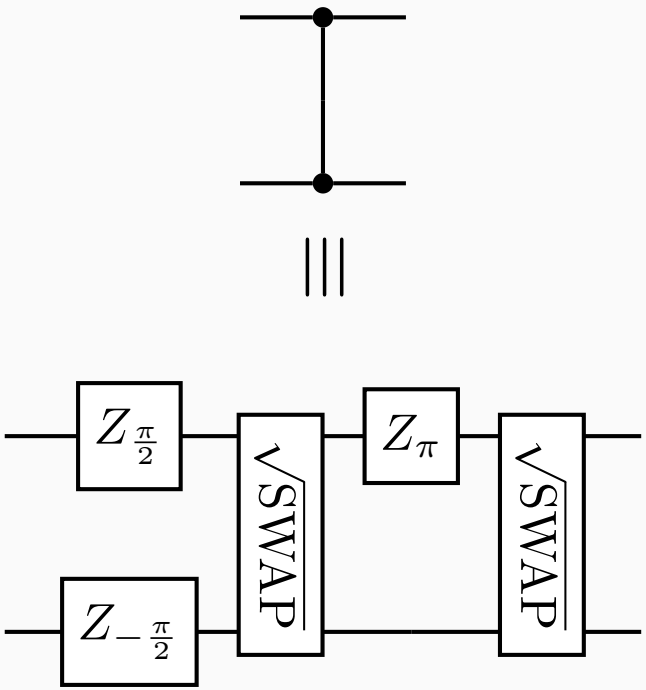
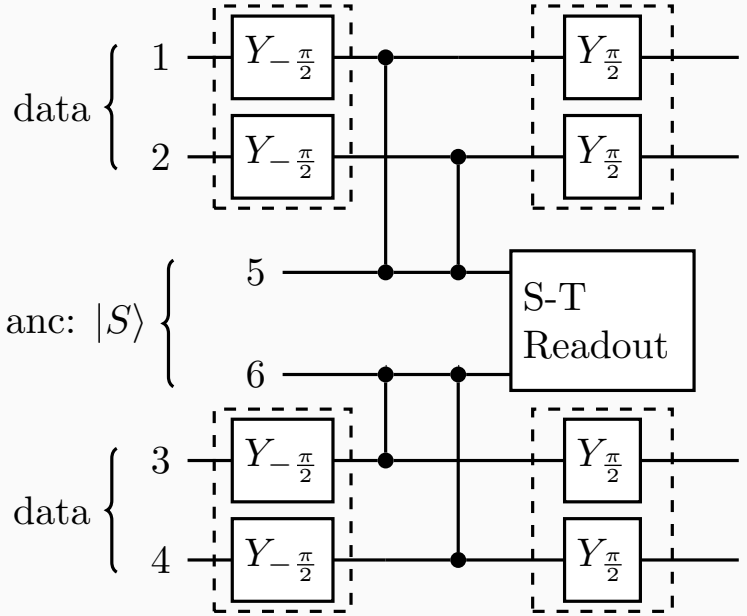


(a) CZ decomposition



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Error Model

- **Two-qubit gate:** Each CZ contains two $\sqrt{\text{SWAP}}$. Each $\sqrt{\text{SWAP}}$ has probability $\frac{p_2}{2}$ of having a SWAP error.

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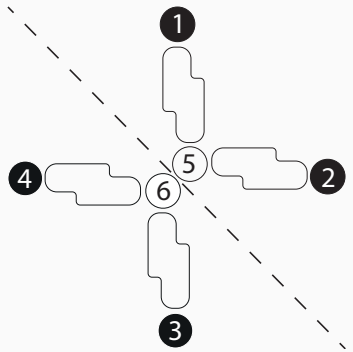

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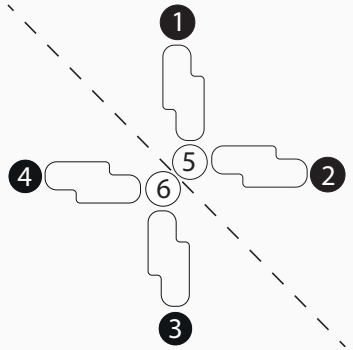
- **Leakage event:** p_{leak} is the probability of a leakage happens during a CZ gate $\Rightarrow$ each half of the stabiliser check will have $2p_{leak}$ probability to get depolarised.



Now Finding The Quantum Error Threshold

If the error rate of the circuit components is:

- **Above threshold**: more physical qubits will introduce more errors $\Rightarrow$ ineffective error correction.
- **Below threshold**: more physical qubits can offer more protections for the logical qubits $\Rightarrow$ effective error correction.

Threshold result

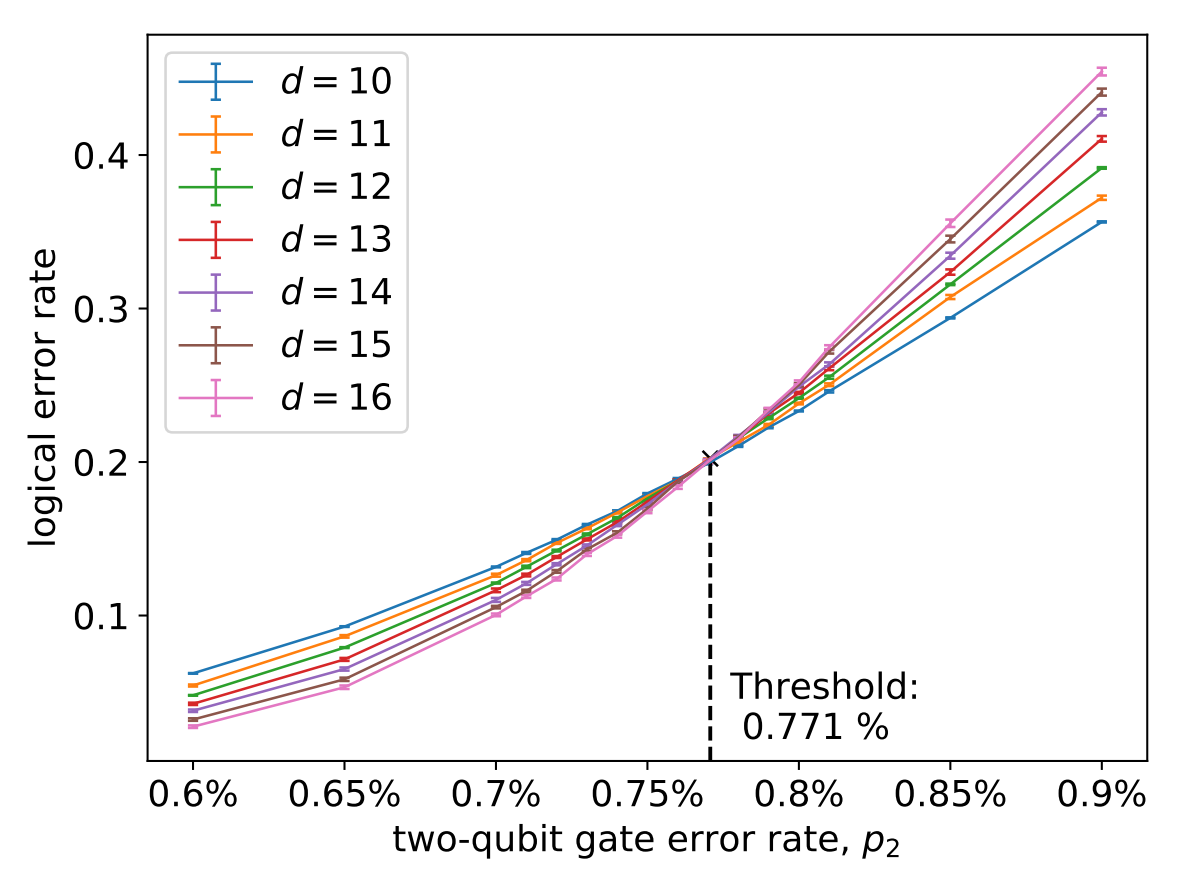


Figure 5: The threshold of the gate errors in the absence of leakage errors $\sim 0.77\%$, which is comparable to the $0.5 \sim 1\%$ of the standard surface code thresholds.

Threshold result

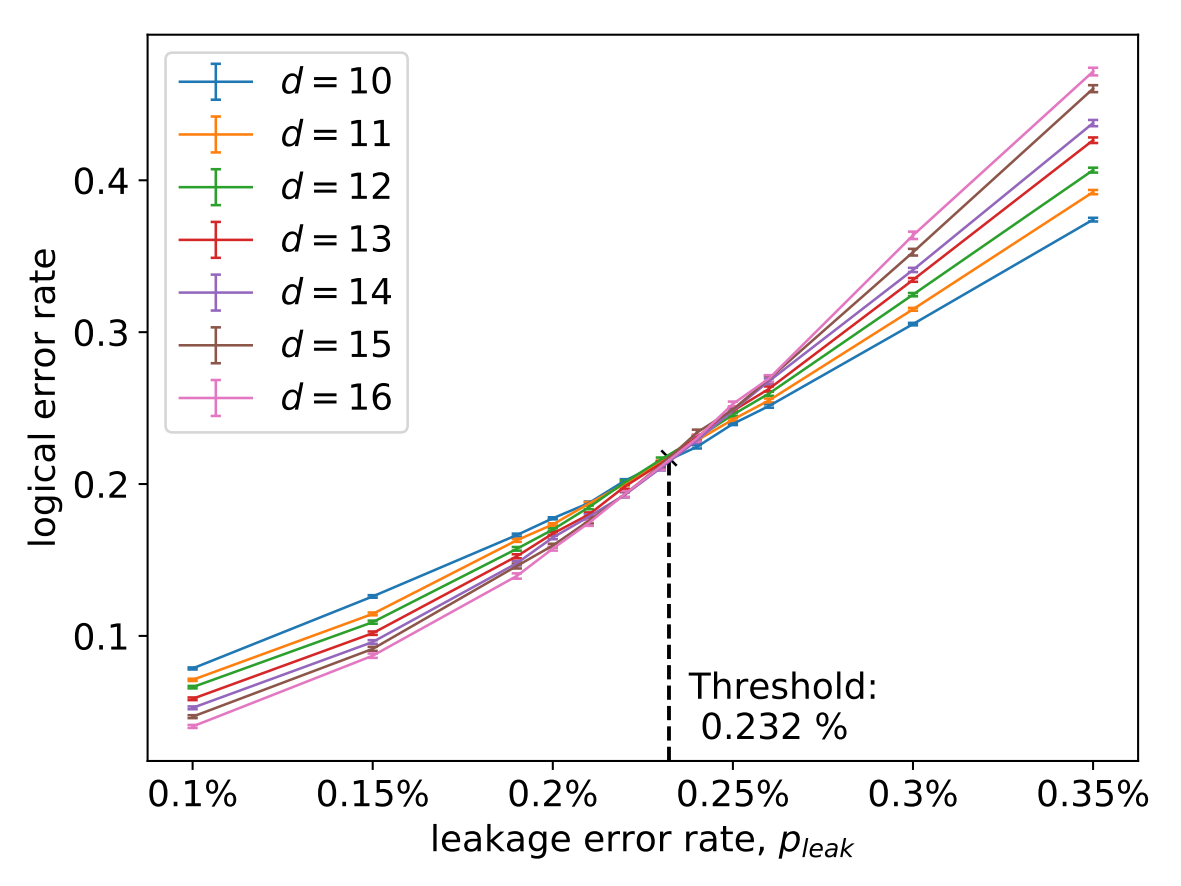


Figure 6: The threshold of leakage error with fixed two-qubit gate error rate ($p_2 = 0.5\%$) is $p_{leak} \sim 0.23\%$. The leakage error threshold can reach $\sim 0.66\%$ in the absence of gate error ($p_2 = 0\%$).

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- Our architecture can be a practical way to implement scalable surface code in silicon structure.
- Leakage errors are highly hardware-dependent.
  $\Rightarrow$ Most effective solution: likely to be hardware-based.